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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/729,239

12/05/2003

Gary L. Swoboda

TI-34656

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7590

06/26/2006

TEXAS INSTRUMENTS INCORPORATED

P O BOX 655474, M/S 3999

DALLAS, TX 75265

EXAMINER

CHERRY, STEPHEN J

ART UNIT

PAPER NUMBER

2863

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,239	SWOBODA, GARY L.	
	Examiner	Art Unit	
	Stephen J. Cherry	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 7-11 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims merely manipulate information without producing a tangible result, therefore they are drawn to non-statutory subject matter.

Claim Objections

Claims 1-6 are objected to because of the following informalities:

The use of the symbol, “/”, renders the claims indefinite because it is not clear whether the symbol is intended to mean “or” or “and”, with respect to the adjacent structures. Appropriate correction is required.

Claims 13-14 are objected to because of the following informalities:

The recitation, “first” and “second” control signals, lacks antecedent basis in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

Art Unit: 2863

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, and 4-15 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,859,891 to Edwards et al.

With regard to claim 1, Edwards discloses a trace apparatus comprising:
a trigger unit responsive to user and target processor state input signals, the trigger unit generating control signals in response to the input signals ('891, col. 8, line 8 and fig. 1, ref. 103);
timing trace apparatus, the timing trace apparatus responsive to control signals for selectively providing timing trace streams during secondary code execution ('891, col. 8, line 58);
program counter/data trace apparatus, the program counter/data trace apparatus responsive to signals from the control apparatus for selectively providing program counter/data trace streams during secondary code execution when the timing trace unit is providing signal during the secondary code execution ('891, col. 6, line 45).

With regard to claim 2, and in view of the rejection of claim 1 above, Edwards discloses a apparatus as recited in claim 1 wherein secondary code execution is background/interrupt service routine code execution ('891, including col. 7, line 38, "multitasking", and col. 5, line 59, describing providing information in a manner that does not affect normal pipeline performance.

With regard to claim 3, and in view of the rejection of claim 1 above, Edwards discloses a trace apparatus as recited in claim 1 wherein the target processor is can have one of an unprotected pipeline and a protected pipeline ('891, col. 5, line 62).

With regard to claim 5, and in view of the rejection of claim 1 above, Edwards discloses a trace apparatus as recited in claim 1 where in the target processor has three states, a primary code execution state ('891, col. 5, line 62, "pipeline" operation), a secondary code execution state ('891, col. 5, line 62, operation of debug circuit that does not affect "pipeline" operation), and an execution halt state ('891, fig. 2, ref. 211 and 212).

With regard to claim 6, and in view of the rejection of claim 1 above, Edwards discloses a trace apparatus as recited in claim 5 wherein the timing trace stream can be controllably enabled during an execution halt state ('891, col. 8, line 44).

With regard to claim 7, Edwards discloses a method of controlling trace streams in a target processor, the method comprising:
generating a timing trace stream in the target processor in response to preselected user and target processor input signals ('891, col. 8, line 61 "timing information"); and
when the timing trace stream is being generated, generating a program counter and a data trace stream in response to predetermined user and target processor input signals '891, col. 8, line 58).

With regard to claim 8, and in view of the rejection of claim 7 above, Edwards discloses a method as recited in claim 7 further comprising including in the target processor input signals indicia of the state of the target processor, the target processor

Art Unit: 2863

having a primary code execution state, a secondary code execution state and an execution halt state ('891, col. 9, line 66).

With regard to claim 9, and in view of the rejection of claim 7 above, Edwards discloses a method as recited in claim 7 further comprising including in the target processor input signals indicia indicating whether the target processor was in a protected pipeline mode of operation or in an unprotected pipeline mode of operation ('891, col. 9, line 66, "stall" signal refers to pipeline mode of operation).

With regard to claim 10, and in view of the rejection of claim 7 above, Edwards discloses a method as recited in claim 7 further comprising including in the user input signals whether the timing trace was enabled during instruction execution halts ('891, col. 8, line 61, and col. 10, line 64).

With regard to claim 11, and in view of the rejection of claim 9 above, Edwards discloses a method as recited in claim 9 further comprising including in the user input signals whether the timing trace stream was enabled during the secondary code execution state ('891, col. 8, line 61, and col. 10, line 64).

With regard to claim 12, Edwards discloses a processing unit comprising: a central processing unit, the central processing unit having three states of operation, a primary code execution state, a secondary code execution state and an execution halted state ('891, fig. 2, ref. 102, depicts processor, col. 5, line 62, "pipeline" operation, col. 5, line 62, operation of debug circuit that does not affect "pipeline" operation, and fig. 2, ref. 211 and 212, showing stall feature or pipeline); and trace generating apparatus

Art Unit: 2863

including program counter generation and a data trace stream generation unit, the program counter trace stream generation unit and the data trace generation unit responsive to control signals for generating the program counter and the data trace streams respectively ('891, fig. 4, 402); a timing trace stream generation unit, the timing trace stream generation unit generating a timing trace stream in response to control signals; and a trigger unit responsive to user input signals and to central processing unit signals for generating control signals controlling the timing trace generation unit and the program counter and data trace generation unit ('891, col. 8, line 58).

With regard to claim 13, and in view of the rejection of claim 12 above, Edwards discloses a processing unit as recited in claim 12 wherein first control signals enable the timing trace generation unit during the secondary code execution state ('891, col. 8, line 8, and col. 9, line 66).

With regard to claim 14, and in view of the rejection of claim 13 above, Edwards discloses a processing unit as recited in claim 13 wherein second control signals enable the timing trace generation device and the program counter and data trace generation units during the secondary code execution ('891, col. 8, line 8, and col. 9, line 66).

With regard to claim 15, and in view of the rejection of claim 12 above, Edwards discloses a processing unit as recited in claim 12 including indicia of a protected pipeline mode of operation and of an unprotected mode of operation of the central processing unit are part of the central processing unit input signals ('891, fig. 4, "stalled", 410, indicates whether pipeline is protected from overfilling buffer).

Allowable Subject Matter

Claim 4 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if the objection of the base claim described above is overcome.

The following is a statement of reasons for the indication of allowable subject matter:

Claim 4 recites, "a pipeline flattener, the pipeline flattener aligning the program counter address with the completion of the instruction, the pipeline flattener flushing instructions in response to a halt execution signal in an unprotected pipeline, the pipeline flattener halting operation in a protected pipeline". This feature, in combination with the remaining structure, overcomes the prior art of record.

Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen J. Cherry whose telephone number is (571) 272-2272. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2863

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SJC



MICHAEL NGHIEM
PRIMARY EXAMINER